

Amendments to the Specification:

Please replace the paragraph beginning on page 8, line 19, with the following amended paragraph:

I/O ports ~~302-402~~ also comprise east line card 306 that interfaces signals to/from the "east" side 208 of node 101-3. East line card 206 receives an OC-768 signal from node 101-2 on line 111-2-3, in this exemplary embodiment, and transmits an OC-768 signal to node 101-2 on line 112-3-2. East line card 306 performs optical/electrical conversion, retiming, signal replication and other well-known functions, as will be described in more detail below, in connection with FIG. 6.

Please replace the paragraph beginning on page 8, line 24, with the following amended paragraph:

Further, I/O ports ~~302-402~~ comprise a plurality of trib cards 308. There are 8 trib cards, 308-1 through 308-8, in this exemplary embodiment. Each trib card 308-1 through 308-8 receives/sends two OC-192 trib signals. Other arrangements of trib cards 308 may be implemented by those skilled in the art after reading this specification. An exemplary trib card 308 will be described further, below, in connection with FIG. 7.

Please replace the paragraph beginning on page 8, line 29, with the following amended paragraph:

I/O ports ~~302-402~~ are connected to both switch core 202-3-A and 202-3-B via a ~~backplane, backplane 312,~~ which will be described in more detail in connection with FIGS. 5, 11 and 12, below. Logically, and in accordance with the description of FIG. 2, above, west line card 304 receives an OC-768 signal from node 101-4 on line 111-4-3 and transforms the optical signals into electrical signals, conditions the signals for use in node 101-3 and send them to north switching network 201-3-N along unidirectional 40 Gb/s line 410, according to this embodiment of this invention. North switching network

201-3-N performs add/drop multiplexing, switching and timeslot interchanging, as described above. North switching network 201-3-N sends an output signal to east line card 306 on unidirectional 40 Gb/s line 412. East line card 306 transforms the electrical signals into optical signals and sends them to node 101-2 on line 111-3-2.

Please replace the paragraph beginning on page 10, line 25, with the following amended paragraph:

FIG. 5 depicts a block diagram of physical connections between I/O ports 402 and switch cores 202-3-A and 202-3-B across an exemplary backplane 314 (shown in partial view) of node 101-3 according to an aspect of this invention. Line cards 304 and 306 and trib cards 308-1 through 308-8 are connected to a backplane ~~402-314~~. Backplane ~~402-314~~ comprises a plurality of uni-directional traces that carry electrical signals between the I/O ports ~~302-402~~ and switching cores 202-3-A and 202-3-B of node 101-3. In this exemplary embodiment of physical connections, west line card receives an OC-768 from node 1014 on line 1114-3 and transmits an OC-768 signal to node 101-2 on line 112-34. West line card performs optical/electrical conversion, retiming and signal replication to effect redundancy.

Please replace the paragraph beginning on page 11, line 3, with the following amended paragraph:

West line card 304 sends identical copies of the received OC-768 signal into backplane ~~402-314~~ to switch core 202-3-A on line trace 301-A and to switch core 202-3-B on line trace 301-B. These signals are processed by switch core 202-3-A and switch core 202-3-B and delivered to east line card 306 on line traces 312-A and 312-B, respectively. East line card 306 selects one of the signals, performs electrical/optical conversion and sends the resulting optical signal on line 111-3-2 to node 101-2.

Please replace the paragraph beginning on page 11, line 16, with the following amended paragraph:

A plurality of trib cards 308-1 through 308-8 are connected to backplane ~~402-~~
314. Only trib card 308-1 and trib card 308-8 are illustrated here for clarity. Each trib card 308-1 through 308-2 receives an OC-192 signal on trib 121-3-1 through 121-3-8 and a second OC-192 signal on trib 121-3-9 through 121-3-16, respectively.

Please replace the paragraph beginning on page 12, line 15, with the following amended paragraph:

Furthermore, trib card 308-8 receives an OC-192 signal on trib 121-3-16 performs optical/electrical conversion, retiming and signal replication and then transmits identical signals on trib trace 334-16-I (wherein "16" stands for "trib16" and "I" stands for "input") to switch core 202-3-A and on trib trace 335-16-I to switch core 202-3-B. Switch core 202-3-A and switch core 202-3-B perform their switching functions on the input signals and send output signals to trib card 308-8 on trib trace 334-16-O (wherein "O" stands for "output") and trib trace 335-16-O, respectively. Trib card 308-8 selects one of the signals, performs electrical/optical conversion and sends the resulting signal on trib 122-3-16. Further detail of backplane ~~402-~~314 will be described further, below, in connection with FIGS. 10-12.

Please replace the paragraph beginning on page 12, line 24, with the following amended paragraph:

Turning to FIG. 6, west line card 304 is illustrated in more detail. According to this exemplary embodiment, west line card receives an OC-768 signal from optical line 111-4-3 at optical/electrical transceiver 502. Optical/electrical transceiver 502 performs optical to electrical conversion as is known in the art and transmits the resultant electrical signals over 16 bit bus 504 at 2.5 Gb/s to transceiver 506. Transceiver 506 performs deserialization and timing functions as is known in the art and transmits the resultant

electrical signals over 32 bit bus 508 at 1.25 Gb/s. Eight bits of bus 508 are delivered to each of four loop-back transceivers 510-1 through 4. In this exemplary embodiment of this invention, loop-back transceivers 510-1 and 510-2 comprise one integrated circuit 512-1 and loop back transceivers 510-3 and 510-4 comprise a second integrated circuit 512-2. Loop back transceivers 510-1 through 4 each receive 8 bit from transceiver 506 and transmits 4 bits (16 bits total) at 2.5 Gb/s across backplane ~~402~~314 to switch core A, north on trace 310-A and to switch core B, north on trace 310-B.

Please replace the paragraph beginning on page 13, line 12, with the following amended paragraph:

Turning to FIG. 7, east line card 306 is illustrated in more detail. According to this exemplary embodiment, east line card 306 receives an OC-768 signal from optical line 112-2-3 at optical/electrical transceiver 602. Optical/electrical transceiver 602 performs optical to electrical conversion as is known in the art and transmits the resultant electrical signals over 16 bit bus 604 at 2.5 Gb/s to transceiver 606. Transceiver 606 performs deserialization and timing functions as is known in the art and transmits the resultant electrical signals over 32 bit bus 608 at 1.25 Gb/s. Eight bits of bus 608 are delivered to each of four loop-back transceivers 510-5 through 8 (all loop-back transceivers 510 are identical according to this exemplary embodiment of this invention). In this exemplary embodiment of this invention, loop-back transceivers 510-6 and 510-7 comprise one integrated circuit 512-3, and loop back transceivers 510-7 and 510-8 comprise a second integrated circuit 512-4. Loop back transceivers 510-5 through 8 each receive 8 bit from transceiver 606 and transmits 4 bits at 2.5 Gb/s across backplane ~~402~~314 to switch core A, south on trace 314-A and to switch core B, south on trace 314-B.

Please replace the paragraph beginning on page 14, line 12, with the following amended paragraph:

Loop back transceiver 710-1 delivers 4 bits at 2.5 Gb/s over backplane ~~402~~314 to switch A, north on trace 320-1-I and 4 bits at 2.5 Gb/s over backplane ~~402~~314 to switch

B, north on trace 321-1-I. Loop back transceiver 710-2 delivers 4 bits at 2.5 Gb/s over backplane ~~402-314~~ to switch A, south on trace 320-9-I and 4 bits at 2.5 Gb/s over backplane ~~402-314~~ to switch B, south on trace 320-9-I.

Please replace the paragraph beginning on page 25, line 5, with the following amended paragraph:

West line card 304 sends identical copies of line 111-4-3's OC-768 signal into backplane ~~402-314~~ to north switching network 201-3-N in switch core 202-3-A on line trace 410-A and to north switching network 201-3-N in switch core 202-3-B on line trace 410-B. These signals are processed by north switching network 201-3-N in switch core 202-3-A and north switching network 201-3-N in switch core 202-3-B and delivered to east line card 306 on line traces 312-A and 312-B, respectively. East line card 306 selects one of the signals, performs electrical/optical conversion and sends the resulting optical signal on line 111-3-2 to node 101-2.

Please replace the paragraph beginning on page 25, line 12, with the following amended paragraph:

Additionally, dual line card 304 west sends identical copies of OC-768 signals from line 1011-4-3's into backplane ~~402-314~~ to north switching network 201-3-N in switch core 1102-3-A on line trace 1210-A and to north switching network 201-3-N in switch core I 102-3-B on line trace 1210-B. These signals are processed by north switching network 201-3-N in switch core 1102-3-A and north switching network 201-3-N in switch core 1102-3-B and delivered to east line card 306 on line traces 1212-A and 1212-B, respectively. East line card 306 selects one of the signals, performs electrical/optical conversion and sends the resulting optical signal on line 1011-3-2 to node 1001-2.

Please replace the paragraph beginning on page 26, line 3, with the following amended paragraph:

Returning briefly to FIGS. 11 and 12, there is a plurality of trib cards 308-1 through 308-8 connected to backplane ~~402-~~314. Four quad trib cards and four dual trib cards are illustrated, to show the versatility of the present invention. For purposes of clarity in FIGS. 13 and 14, and for purposes of parallelism with FIG. 5, only quad trib card 308-1 and dual trib card 308-8 are illustrated here. One skilled in the art will be able to design a complete backplane 314 including the connections for all eight trib cards after studying these drawings and the accompanying text.

Please replace the paragraph beginning on page 28, line 31, with the following amended paragraph:

One output of first switching network 1620 comprises 32 bit bus 1642, which delivers eight bits to each of four loop-back transceivers 510-1 through 4. In this exemplary embodiment of this invention, loopback transceivers 510-1 and 510-2 comprise one integrated circuit 512-1 and loop back transceivers 510-3 and 510-4 comprise a second integrated circuit 512-2. Loop back transceivers 510-1 through 4 each receive 8 bit from switching network 620 and transmits 4 bits (16 bits total) at 2.5 Gb/s across backplane ~~402-~~314 to north switching network of switch core 202, north on trace 410-A and to switch core B, north on trace 410-B.

Please replace the paragraph beginning on page 29, line 6, with the following amended paragraph:

One output of second switching network 1622 comprises 32 bit bus 1644, which delivers eight bits to each of four loop-back transceivers 510-1 through 4. In this exemplary embodiment of this invention, loop-back transceivers 510-1 and 510-2 comprise one integrated circuit 512-1 and loop back transceivers 510-3 and 510-4 comprise a second integrated circuit 512-2. Loop back transceivers 510-1 through 4 each

receive 8 bit from switching network 1622 and transmits 4 bits (16 bits total) at 2.5 Gb/s across backplane ~~402-314~~ to switch core 1102-A, north on trace 1210-A and to switch core 1102-B, north on trace 1210-B.

Please replace the paragraph beginning on page 30, line 27, with the following amended paragraph:

Loop back transceiver 710-1 delivers 4 bits at 2.5 Gb/s over backplane ~~402-314~~ to switch A, north on trace 320-1-I and 4 bits at 2.5 Gb/s over backplane ~~402-314~~ to switch B, north on trace 321-1-I. Loop back transceiver 710-2 delivers 4 bits at 2.5 Gb/s over backplane ~~402-314~~ to switch A, south on trace 320-9-I and 4 bits at 2.5 Gb/s over backplane ~~402-314~~ to switch B, south on trace 320-9-I. Loop back transceiver 710-3 delivers 4 bits at 2.5 Gb/s over backplane ~~402-314~~ to switch A, north on trace 1220-1-I and 4 bits at 2.5 Gb/s over backplane ~~402-314~~ to switch B, north on trace 1221-1-I. Loop back transceiver 710-2 delivers 4 bits at 2.5 Gb/s over backplane ~~402-314~~ to switch A, south on trace 1220-9-I and 4 bits at 2.5 Gb/s over backplane ~~402-314~~ to switch B, south on trace 1220-9-I.